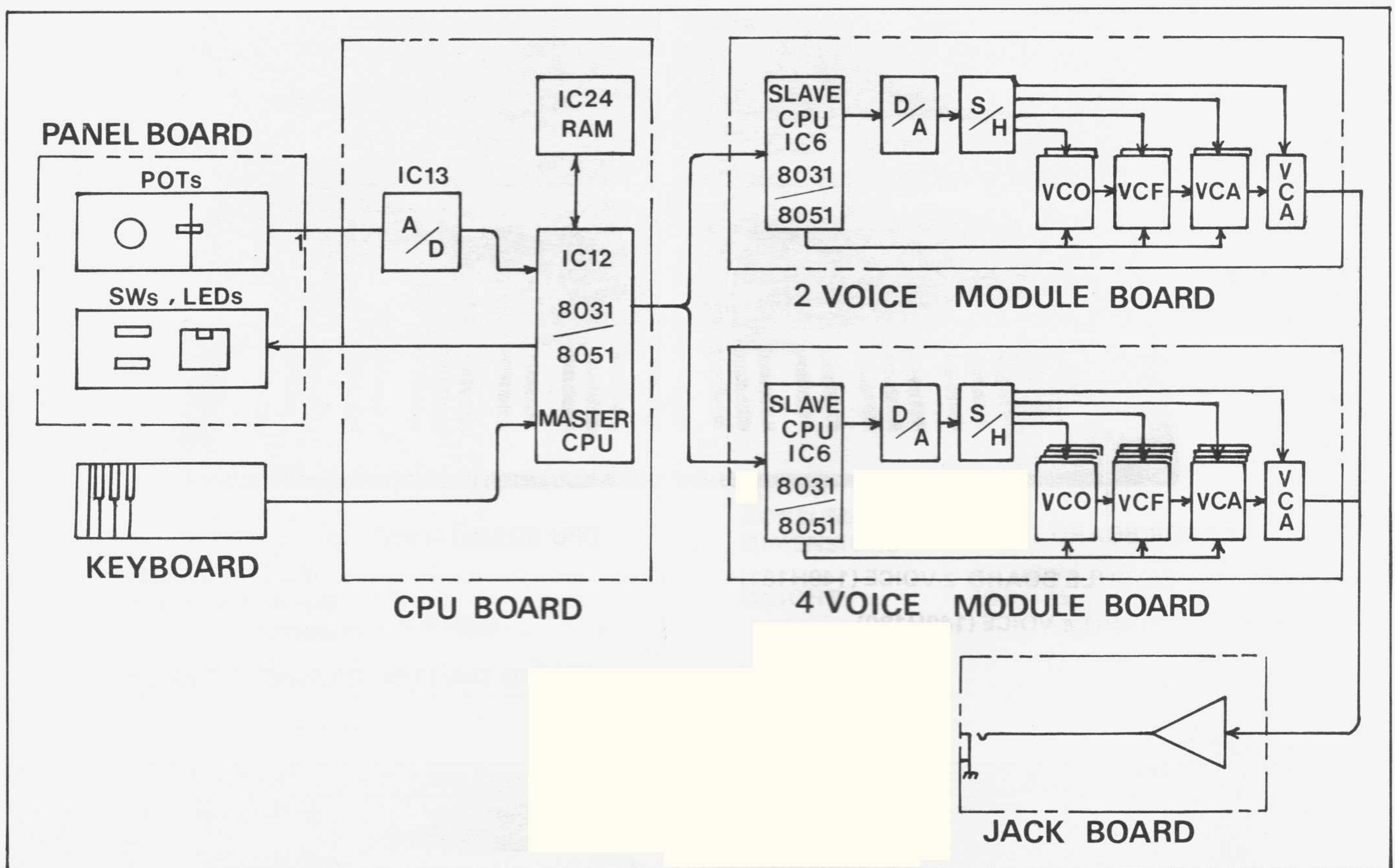


# CIRCUIT DESCRIPTION

## General



The setting values of the potentiometers on the **PANEL BOARDs** are converted into digital equivalent by the A/D converter (IC13) on the **CPU BOARD**, and are read by the **MASTER CPU** (IC12). The setting values of the switchies on the **PANEL BOARDs** are directly read by the CPU through the Matrix circuits divided into the two **PANEL BOARDs**. The CPU (IC12) writes these data into **RAM** (IC24). The data in the **RAM** are read by control operation through the panel when required and

are fed to the CPUs (**SLAVE CPU**s) on the **MODULE BOARDs** in serial format.

The **SLAVE CPU**s control **VCO**s, **VCF**s and **VCA**s using the data (tone data, keyboard information, etc.) coming from the **MASTER CPU**.

The **BENDER** and foot pedal controls are processed by analog circuits. The **SLAVE CPU**s gate the right analog switches to pass these control voltages to individual destinations to introduce additional features.

## MASTER CPU

IC12 (CPU BOARD) P8031/P8051/P8051-318

Difference Between CPUs

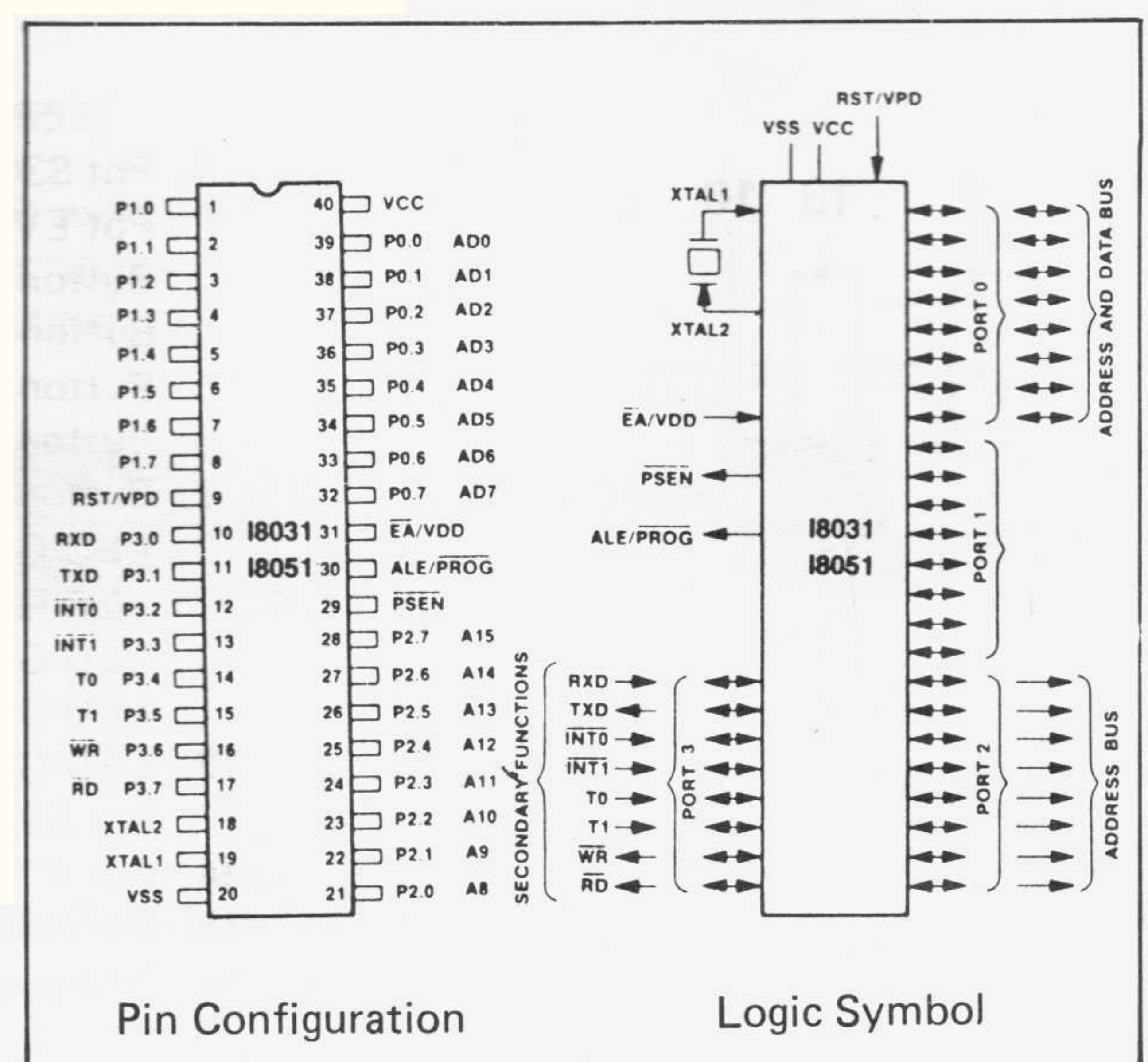
**P8031** . . . . .for early products, associated with **PROM IC26** containing the operational program exclusive to the **JP-6**.

**P8051** . . . . .tentatively used. To be handled as **P8031**.

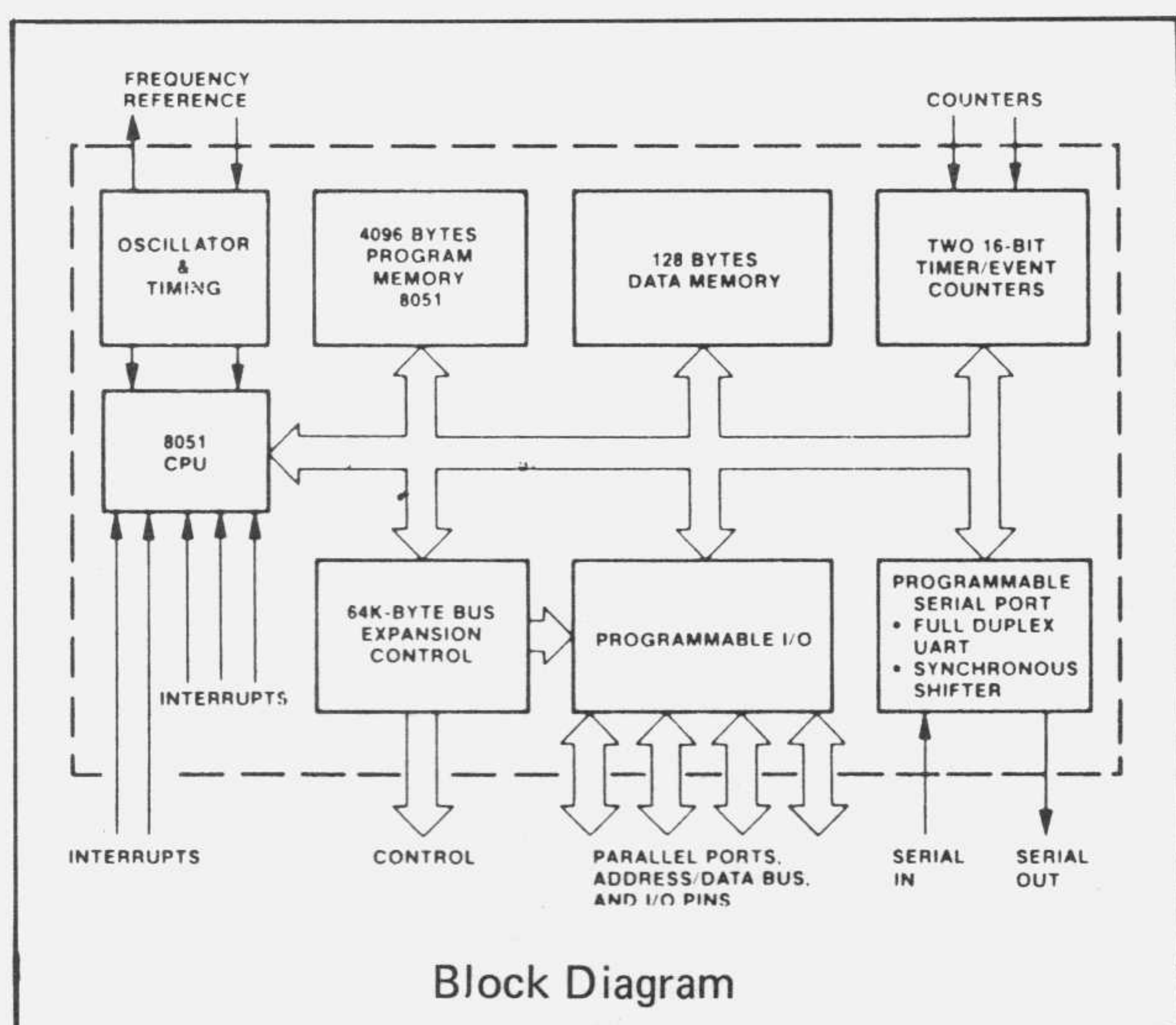
**P8051-318** . . . . .contains the program in the on-chip **ROM**, making **IC26** redundant.

## Compatibility

Three CPUs function the same as long as external **PROM IC26** is enabled. Pulling up **EA** (pin 31) of **P8051-318** will change programs from external to internal (see CPU circuit diagram), but this is unnecessary when **IC26** operates perfectly.

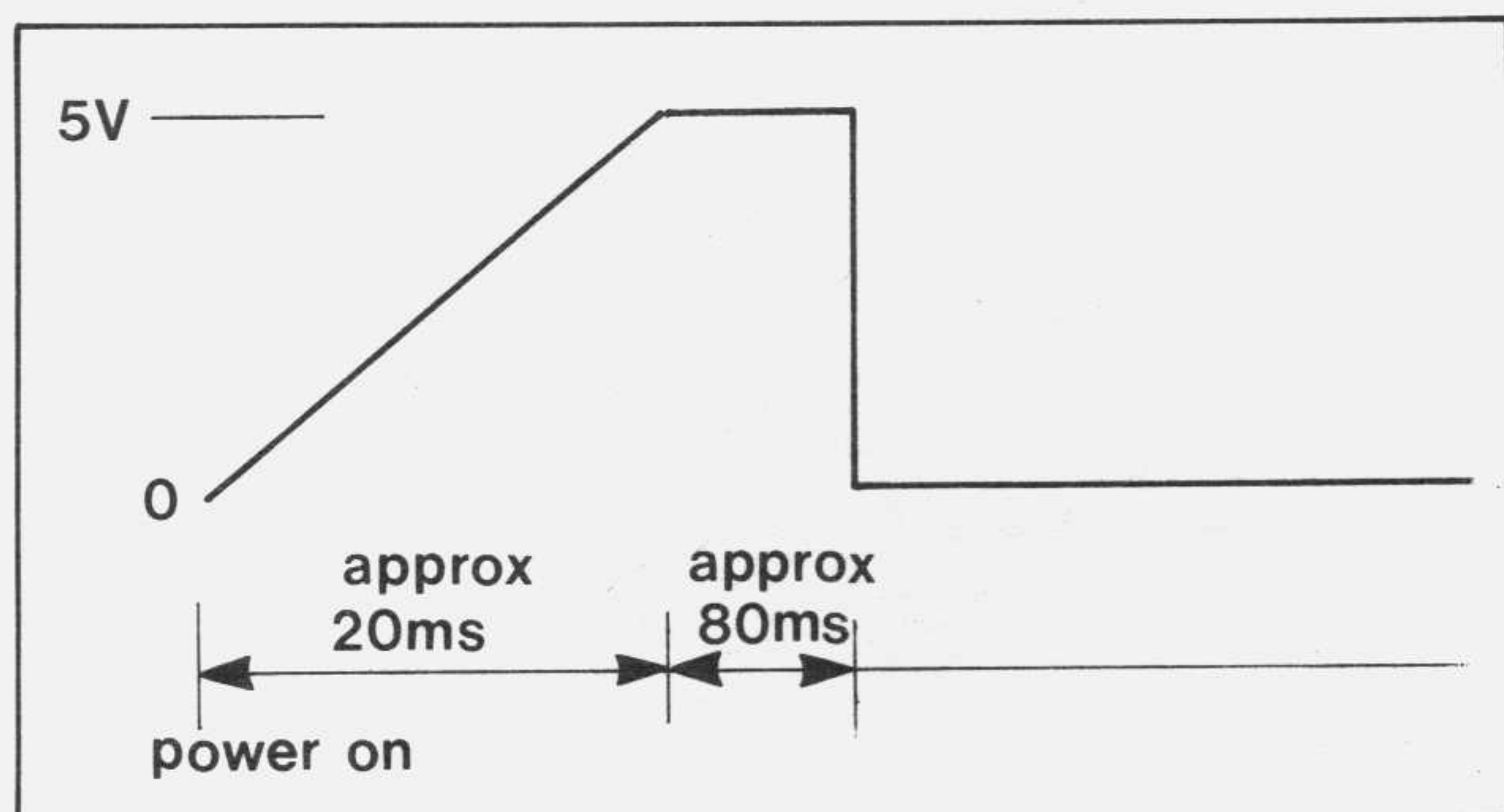






### Pin Function

**RST**..... The level of the reset terminal is kept high by RESET circuit (TR6, TR7, TR8 and IC21) for more than 24 clocks after the DC voltages becomes stable.



**P0**..... carries data and address data.

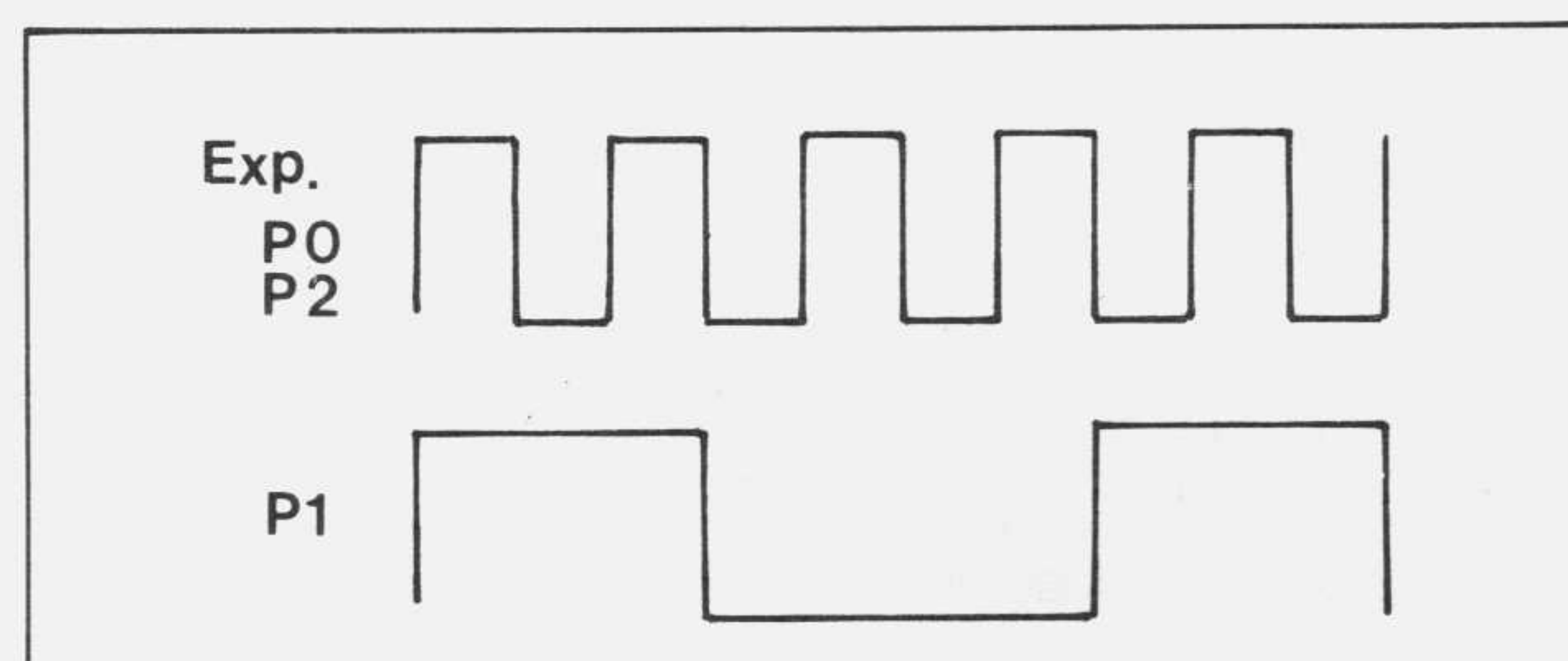
**ALE**..... sends latch clock to IC17 to latch address off the P0 bus.

**PSEN**..... enables IC26 to read a program in the PROM through the P0 bus.

**P1**..... serves as an I/O port.

It presents panel LED lighting, potentiometer and switch reading addresses.

**P2**..... issues addresses



**RD**..... enables Read Address Decoder IC19 when the CPU wants to read necessary data. IC19 decodes select signals (P2.4-P2.6) and directs either of IC13, IC14, IC23, IC24, IC25 or IC27 to place data on the data bus.

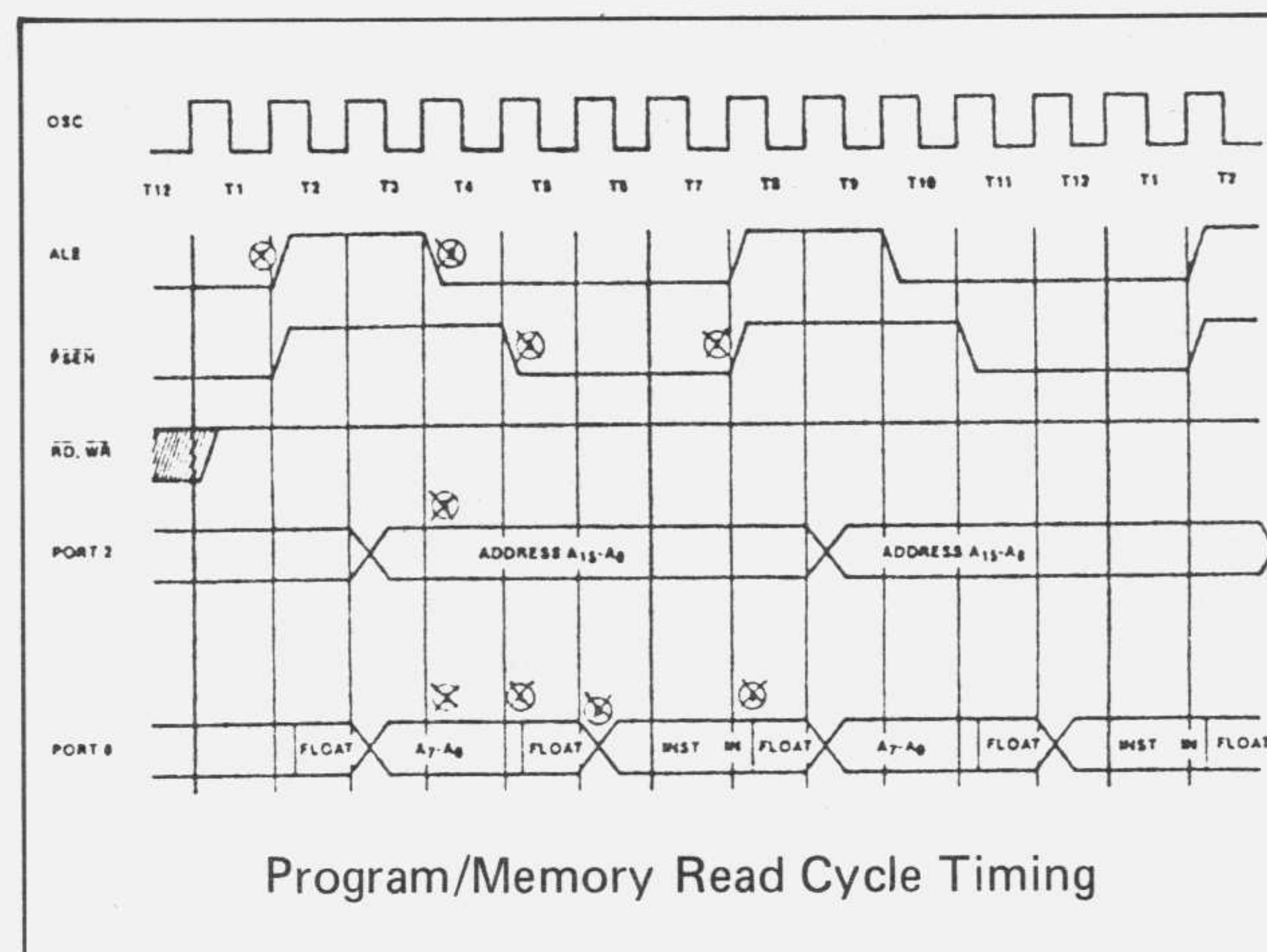
**WR**..... enables Write Address Decoder IC18 which, upon decoding address being fed, clocks RAMs, A/D converter (IC13) and LED driver (IC15, IC16).

**T0, T1, TX**..... transmit data to the cassette tape interface, MIDI bus and SLAVE CPUs.

**RX**..... reads data from MIDI bus.

**INT 1**..... reads data from the cassette interface.

**INT 0**..... not used.

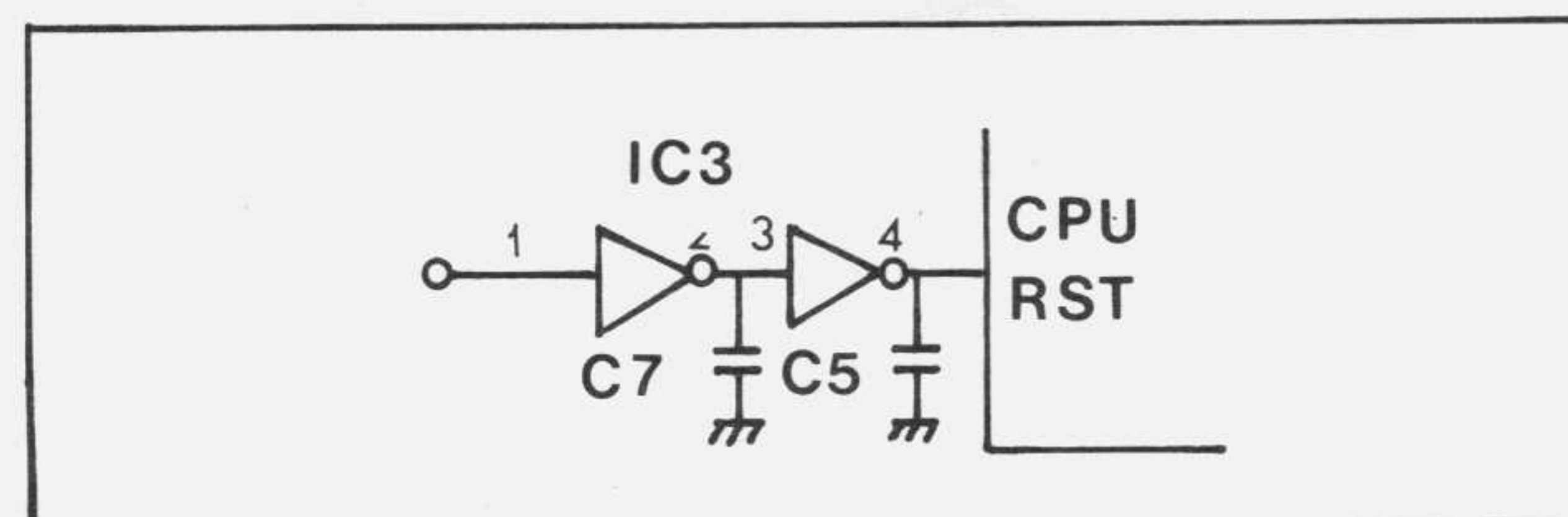


### SLAVE CPU

#### IC6 (MODULE BOARD)

**Compatibility** .. In the same way as IC12 on the CPU BOARD, P8031, P8051 or P8051-319 is used for the CPU (IC6). Refer to "MASTER CPU." P8051-319 makes IC1 and IC5 redundant.

**RST**..... receives a shaped reset pulse from the CPU BOARD through buffers. The buffers (IC3) and capacitors (C5 and C7) effectively protect the CPU against static charge.



**P0, P2, PSEN**.... Refer to the description in the and ALE MASTER CPU section.

**P1**..... delivers addresses to the S/H analog switches.

**RD** and **INT 1**.. clock the address latches (IC7, IC8) to ON or OFF analog switches.

**INT 0**..... reads the frequencies of the VCOs during compute operation.

**RX**..... accepts data from the MASTER CPU.

**TX**..... goes high during Compute, signaling MASTER CPU not to send data.

**T0, T1**..... transmit LFO-LED lighting signals, and transmit and receive LFO sync pulses to and from the other SLAVE CPU.