NOTE: The F4013 version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4013 TRUTH TABLES

<table>
<thead>
<tr>
<th>SYNONRONOUS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP</td>
<td>D</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>J</td>
<td>H</td>
</tr>
</tbody>
</table>

Conditions: SD = CP = LOW

ASYNCHRONOUS

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD = LOW</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>
| Qt+1 = State After Clock Positive Transition

F4001 QUAD 2-INPUT NOR GATE

F4001 LOGIC AND CONNECTION DIAGRAM (DIP (TOP VIEW))
SPECIFICATIONS

OUTPUT IMPEDANCE
H: 220k ohms  L: 10k ohms

OUTPUT LEVEL
H: 3.5Vpp into 220k
L: 5.5Vpp into 10k
(Vol. ACC. max)
TRIGGER: +15V

EXT. CLOCK
+5V--- +15V
min. 5ms in length

POWER CONSUMPTION
9W (117V)
13W (220/240V)

DIMENSIONS
300(W)x280(D)x250(H) mm
11.8 x 11.0 x 8.1 in

NET WEIGHT
5.5Kg  12.1 lbs
EXT. CLOCK CIRCUIT:
independent of OP-104
S/N up to 780699, mounted
on OP-129.

LOGIC Board GL-9

FUSES RATING

<table>
<thead>
<tr>
<th>F1 (-5V)</th>
<th>F2 (+15V)</th>
<th>F3 (+5V)</th>
<th>F4 (prim.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGA 0.125A (008-022)</td>
<td>SGA 1A (008-026)</td>
<td>SGA 0.5A (008-024)</td>
<td>SGA 0.5A (008-024)</td>
</tr>
<tr>
<td>CEE T50mA (008-053)</td>
<td>CEE T250mA (008-060)</td>
<td>CEE T400mA (008-062)</td>
<td>CEE T250mA (008-060)</td>
</tr>
</tbody>
</table>
CR-78 CIRCUITS TIMING DIAGRAM

T1

CPL (Master osc reset)

TO (Master output)

Decoder 0, 5, 9

Decoder 7

Decoder 8

Decoder 11-14

(7, 16 = H level) (12 and 13 are output only after "START")

Decoder 6

Decoder 7

Decoder 9

Decoder 10

WRITE Switch

Flow Chart

Program Rhythm Selector

OFF

ON

Decoders:

Decoder 0

Decoder 1

Decoder 2

Decoder 3

Decoder 4

Decoder 5

Decoder 6

Decoder 7

Decoder 8

Decoder 9

Decoder 10

Decoder 11

Decoder 12

Decoder 13

Decoder 14

Decoder 15

Other pins' condition are the same as shown in "off".

Program Rhythm Selector

OFF

ON

Decoders:

Decoder 0

Decoder 1

Decoder 2

Decoder 3

Decoder 4

Decoder 5

Decoder 6

Decoder 7

Decoder 8

Decoder 9

Decoder 10

Decoder 11

Decoder 12

Decoder 13

Decoder 14

Decoder 15

1 cycle

4ms

1 cycle

3ms

10ms (TEMPO full clockwise)

10ms
One chip microcomputer //PD8048C—015

The µPD8048 is an 8-bit parallel computer fabricated on a single silicon chip. The 8048 contains a 1k x 8 ROM program memory, a 64 x 8 RAM memory, 27 I/O lines, an 8-bit timer/counter and clock circuits. Used in the CR-78 is a µPD8048C-015 version in which the programs and data dedicated to the CR-78 are stored in program memory.

CR-78 Flow Chart

1. Power on
   ↓
   Initiation

2. Onset of a measure?
   ↓
   YES
   2B
   NO

3. Prepare the next data

4. Read CANCEL SWITCH (Group H)

5. START/STOP SWITCH T1?
   ↓
   H
   L

6. MASTER OSCILLATOR TO?
   ↓
   H
   L

7. WRITE SWITCH INT?
   ↓
   H
   L

8. MASTER OSCILLATOR TO?
   ↓
   H

9. Output data to VOICING and LED circuits

Read VARIATION SWITCH

Read SWITCHES: A to G groups

Read SWITCHES: PROGRAM and INSTRUMENT
Write Rhythm patterns into RAM
CIRCUIT DESCRIPTION

The CR-78 is a computerized rhythm machine whose rhythms are controlled by the resident computer through internally stored programs. Rhythms other than stored can be programmed as desired by using the built-in expansion ROM and RAMs. Sequential program order is outlined in the flow chart and the timing diagram shows relationship among principal circuits waveforms. (see previous page)

The following description is composed of two sections: General Introduction and Detailed Function. Title numbers refer to those in flow chart.

GENERAL INTRODUCTION

1. POWER ON

When power is first applied, two oscillators start oscillation: MASTER OSCILLATOR, determines rhythm tempo, ranging from 5Hz to 100Hz; CLOCK GENERATOR, generates timing pulses for the 8048 in each step cycle.

2. 2B. SWITCH SANNING

Even in the stop mode, the computer needs to store a data on switching status so as to output rhythm patterns immediately after the START/STOP switch is depressed. And also a status data is needed at the beginning of a measure.

The switch reading to obtain a switch set-up data is refereed to as switch scanning.

From Port 2 of 8048, signals are routed through the Decoders IC107 and IC108, and the switch matrix to Port 1. Combination of two port's pins according to switch settings becomes a data on switch status. After a rhythm runs, scanning is done once for each measure.

3. PROCESSING and PREPARING DATA

The 8048 prepares the next data according to the internal program based on switch scanning data.

4. SCANNING CANCEL VOICE SWITCH

Since switch scanning is performed once for one measure during rhythm running, switching during the measure is effective in the subsequent measure. However, "CANCEL VOICE" is scanned every cycle to cancel the unwanted voice at once whenever it is specified.

5. SENSING START/STOP SWITCHING

As long as T1, the START/STOP sensing input terminal of 808048 is kept low, the program routine is not allowed to break loop through 1-5, returning to 1. When the START/STOP switch is pushed while a rhythm stops, T1 is pulled to high to start a rhythm and falls to low when the START/STOP is pushed again (stop)

6. SENSING MASTER OUTPUT FALLING

Although each circuit operates its given task in sequence under the control of timing pulses from the CLOCK GENERATOR, each program step must keep pace with oscillation of the master osc. (rhythm tempo) by sensing the falls and rises of waveforms of the master oscillator.

A program step proceeds to the next step when the master's trailing edge goes to negative.

7. SENSING WRITE SWITCHING

When the WRITE switch is tapped, the write hold circuit IC113 is set, applying high level to INT, and causing program routine to jump to 7B.

7B. WRITING PROGRAM RHYTHM

Scanning signals from 5 and 7 of the decoder IC-108 tell the computer which position of INSTRUMENT and which PROGRAM push switch is selected. Then the data on PROGRAM rhythm are stored into the RAMs IC102 and IC103 under the control of a program from the ROM IC104. The RAMs provide memory size for two measures for each voice.

8. SENSING MASTER RISING

The computer executes a program, synchronizing its step with a rhythm tempo. As soon as T0 receives the rise of a master square, 8048 starts to produce rhythm patterns by sending data and control signals out from Port 1 and 2.

9. OUTPUTTING DATA

The Port 1 this time serves as an output port, feeding data for rhythm patterns (VOICES) and LEDs (TRACK) to the latches IC112-IC116 which selectively latch them in sequence under the control of signals coming from the Port 2 through the Decoder IC107. The computer performs the entire loop once for one cycle of master oscillator and 48 times per measure.
FUNCTION -Detail-

1. POWER ON
Resetting of the START/STOP flip-flop IC109A inhibits a rhythm from running by holding T1 of μPF6048 at low level until the START/STOP switch is first tapped.
When power is on, since the both pins 12 and 13 of IC111A are grounded momentarily, its output (pin 11) level swings to high resetting the RS flip flop IC109A which in turn develops high output at pin 2, setting T1 level to low (through Q5-Q7, IC117A and Q11). Pins 12 and 13 of IC111 will go positive as Q103 charges, but IC109A output is kept high until the START/STOP switch is depressed.

2. NO DETAIL

2B. SWITCH SCANNING
Switch scanning cycle initiates to generate internally programed binary signals from the Port 2, P24-P27, feeding them to IC108, binary-to-hexadecimal decoder, from which decoded signals are routed to respective switch groups. From the decoder only one pin outputs negative going pulse while the rest pins output H, and the next pin outputs H with the rest L. These outputs of signals occur in sequence within a time interval of microseconds and repeats over and over again every few milliseconds until the START/STOP switch is depressed to run the rhythm. After running, scanning signals are outputted once at the onset of a measure. This means that changing of any switch setting during a measure is ignored by the computer unless switch setting is kept unchanged until the next scanning.
Similarly, changing the MEASURE of VARIATION in AUTO mode will be made into effective only after previously specified measure(s) has passed.

In MANUAL mode, VARIATION change during a measure is enabled at the beginning of the next measure by holding that changing information until the next scanning is performed.
For this purpose the MANUAL VARI hold circuit is used which consists of IC119. When the START/STOP switch is pressed while a rhythm stops, the RS flip flop IC119 (pins 1-6) is reset by a pulse from Q of IC108, switching pin 3 to H and pin 6 to L.

[Diagram of the circuit with labels IC101, IC108, μPF6048, 74LS138, Scanning Signals, Data Bus 8 lines, P27, P26, P25, P24, Port 2, P17, Port 1, P10, Power ON, STOP, START, STOP, FADE IN, FADE OUT, IC109 Pin 4, FF reset, IC109 Pin 2, FF Q, Q7 Emitter, IC101 8048 T1, IC111 Pin 4, Master reset pulse, Q1 Collector, Master Oscillator]
Depressing the MANUAL switch during rhythm running sets the FF IC119A/B, holding pin 6 or pin 13 at H. When a master output goes low, a scanning pulse is generated from 4 of IC108 after inverted by IC121, it is NANDed with pin 13 input, causing pin 11 to develop a negative going pulse which is detected by the 8048 through Pl6, this is MANUAL "ON" information.

After scanning, a reset pulse is applied from 0 of IC108 to pin 2 through the NAND circuit IC119D.

3. NO DETAIL
4. NO DETAIL

5. SENSING START/STOP SWITCHING

The START/STOP FF IC109A receives a positive going pulse each time the START/STOP switch is pushed, switching its output H or L and holding it until the next push is made.

Pushing the START/STOP switch applies a positive pulse to pin 3 of the START/STOP FF IC109A causing it to have a high or low output until the START/STOP switch is pressed again.

The output from the FF is applied through Q5, Q6 and QF-100 to pin 6 of the comparator IC117A which provides a reference voltage at pin 5. When an input to pin 6 of the comparator exceeds the reference voltage of pin 5, the comparator senses it, sending output to:
1. T1 of 8048 to start the rhythm,
2. the master oscillator and 8 and 16 beat dividers IC109B and IC110 through the one shot pulse generator IC111 (pins 1-6) to reset them and to synchronize their starts.

When the voltage at pin 6 of the comparator drops below the reference voltage, low output is applied to T1 to stop the rhythm.

However, if the FADE IN or FADE OUT switch is in closed position, voltage swing at T1 is delayed behind START/STOP switching due to the time constant in the fade circuit. (Detailed later)

6. MASTER OSCILLATOR

The master oscillator output waveform has a duty ratio of over 50%.

When the WRITE switch is tapped, the WRITE FF IC118 is set, applying high output to IN2 pin of 8048 which will go low when the master output fails. This is a "WRITE ON" information to the computer, upon receiving the "write on" information, switch scanning pulses are sent from 5, 7, 9 and 10 of the decoders and associated data are memorized into external RAMs IC102 and IC103. The circuit configuration and function of the WRITE FF are much the same as in the MANUAL FF except for reset timing.

As shown in the figure, whenever the write switch is tapped, as long as it is occured during master's high level period, information is recognized by the computer when the master output
falls, however, if the write switch is tapped during low level period, it is treated as if it was occurred during the next high level period, and then, sound is reproduced, being delayed by \( \frac{1}{2} \) cycle of the master oscillator.

The longer high level period of the master oscillator waveform is intended to compensate for delayed timing of key operation.

7. NO DETAIL

7B. WRITING PROGRAM RHYTHM

As described in section 6, when the write switch is tapped during a measure, information on PROGRAM rhythm are stored in RAMs at the subsequent master square trailing edge, and INT of 8048 receives H input from the write hold circuit which consists of IC118 which functions in the same way as in the MANUAL VARL (in this case reset pulse is fed from pin 14 or \( \frac{7}{2} \) of IC107).

When the write switch is depressed during a measure, H level is applied at INT pin and is held until master falls, this is "write on" information, and the computer detects through switch scanning (pulses from \( \frac{5}{2} \) and \( \frac{7}{2} \) of IC108) which of PROGRAM switches and which position of INSTRUMENT switch is selected.

The selected INSTRUMENT is first stored into RAM, then rhythm patterns are stored.

When the same instrument has been addressed in the RAM track, rhythm patterns being written are added to the patterns previously stored in the RAM and will not be stored in another track independently.

Required bit numbers for two measures are:
4 (PROGRAM) x 4 (INSTRUMENT) x 96 steps (48 x 2) = 1536 bits.

Data transfer to/from RAMs and ROM are performed as follows:

ALE (Address Latch Enable)
This signal occurs once for 15 Clock Generator frequency, that is, 250kHz, and latches address being outputted from DB, through internal program, delivering the latched signals to RAMs and ROM.

ROM (IO104)
Program memory addressed by the address signals from the latches IC105, IC106 and P20 and P21 is fetched when PFBN is low at 2B and 7B of the flowchart.
8. 9. DATA OUTPUT

-LATCH CIRCUITS-

When the program proceeds at data output routine, Port 1 this time acts as an output port since it is a bidirectional port, representing the data through internal program memory or external ROM and RAMS, data are sent from PIO-P17 to IC112-IC116 latch circuits whose clock input pins receive latch signals from port 2 via decoder IC107. When a latch pulse goes positive while a data signal is fed onto the clock pin, the data is latched and sent to the VOICING circuit or LED. When the latched data is for voicing, it is applied after inverted and amplified by a buffer.

There are three kinds of latched outputs, as the master output goes negative, Qs and Q of IC112-IC114 are cleared, maintaining their pulse lengths almost the same as the master wave length.

On the other hand, Qs of IC115 and IC116 are held until the next latch signal comes since these clear pins of IC115 and IC116 are not connected to the master oscillator output.

Note: since the time interval between pulses within the arrows marked by * is 70μs, they are considered to occur at the same time.

**FADE** and **ACCENT**

As described in section 4, the FADE circuits on OP-100 are enabled when the FADE IN and/or FADE OUT switches are turned on to make the rhythm sounds gradually louder (VCA) as a rhythm starts and to stop the rhythm (T1) as sounds die away.

These timings are determined by the RC constants in the FADE circuits.

Accent pulses are also affected by the FADE circuits in amplitude ratio and are mixed with the sound control voltage in the summing amp. IC117 from which incorporate control voltages are sent to the VCA on the VG-11 to control rhythm volume.

**SOUND KILLER**

These circuits "kill" undesired sounds resulted from transient voltages on their way to output:
1. When power is on, Q512 on the VG-11 is not supplied enough collector voltage to amplify a input signal until Q556 charges to some extent.
2. When power is off, Q558 discharges through Q535 and Q532 on the VG-11, grounding pin 1 of VCA IC502.
3. The circuit composed of Q12 and Q13 on the QL-9 is identical and functions in the same manner as the circuits described above, but is used to protect the RAMs and to prevent disorderly running of 8048.
MC14069BCP

DIP (TOP VIEW)

YDD
14 13 12 11 10 9 8
8 7 6 5 4 3 2 1

VSS

PIN CONFIGURATION

A1 - 1 24 Vcc
A2 - 2 23 A3
A3 - 3 22 A1
A4 - 4 21 A0
A5 - 5 20 CE/NIE
A6 - 6 2108/2154 19 VDD
A7 - 7 18 PROGRAM
ILSB A8 - 8 17 Oy ESB
ILBB D6 - 9 16 D6
OY - 10 15 Oy
O1 - 11 14 D1
VDD - 12 13

NOTE 1 PIN 22 MUST BE CONNECTED TO VDD FOR THE 20A

PIN NAMES

An, A0 ADDRESS INPUTS
O - CE, CE0 DATA OUTPUT, INPUTS
CE1 CHIP SELECT/WRITE ENABLE INPUT

HPC4558

TOP VIEW

OUTPUT 1 2 3 4 +V
-INPUT 5 6 OUTPUT
+INPUT 7 -INPUT
-V 8 +INPUT

BA662

TOP VIEW

5 - V
9 + V

AM2706P

BLOCK DIAGRAM

DATA OUTPUT
U8 - C8

OUT PUT BUFFERS

INPUT

DECODER

Y GATING

64 X 128 ROW ARRAY

PIN CONNECTION DURING READ OR PROGRAM

<table>
<thead>
<tr>
<th>MODE</th>
<th>DATA I/O</th>
<th>ADDRESS INPUTS</th>
<th>TYP. W3</th>
<th>VSS</th>
<th>PROGRAM</th>
<th>CE1E</th>
<th>VDD</th>
<th>VCC</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>9,11 (12)</td>
<td>13, 17</td>
<td>18, 21, 23</td>
<td>12</td>
<td>+2</td>
<td>12</td>
<td>21</td>
<td>24</td>
</tr>
<tr>
<td>SELECT</td>
<td>HIGH IMPEDANCE</td>
<td>DON'T CARE</td>
<td>12</td>
<td>DON'T CARE</td>
<td>12</td>
<td>VDD</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>PROGRAM</td>
<td>READ</td>
<td>READ</td>
<td>12</td>
<td>DO</td>
<td>5</td>
<td>VSS</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

μPD5101E-E

PIN CONFIGURATION

A2 1 22 Vcc
A1 2 21 A2
A0 3 20 A3
A4 4 19 CE1
A5 5 18 CE2
A6 6 17 CE3
A7 7 16 CE4
GND 8 15 GND
D1 9 14 D1
D2 10 13 D2
D3 11 12 D3

LOGIC SYMBOL

A2 A1 A0

TRUTH TABLE

<table>
<thead>
<tr>
<th>R2</th>
<th>R1</th>
<th>R0</th>
<th>Rm</th>
<th>Output</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>Not Selected</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>Not Selected</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>Output Selected</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>HIGH</td>
<td>-W</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>X</td>
<td>Output</td>
<td>Read</td>
</tr>
</tbody>
</table>

BLOCK DIAGRAM
GL-9A (142-009A)  
(Etch mask 052-438A)  
Serial No. 780700-821050  
Use GL-9B for replacement

GL-9 only  
Serial no. up to 780699

GL-9 Circuit Board is the same as GL-9A except for portion shown left and following parts are attached on the foil side.

R202, R201, R105, C105

For the decoder (IC112, 113, 115,116) two kinds of logic IC are available; TTL (74LS175, or equiv.) and CMOS (74C175, 14175, or equiv.).

When CMOS type is used as a replacement for TTL, pin 1 of IC115 and IC116 must be connected to +5V supply through a 10k-ohm as shown in below right (R212, R213). When TTL is used, the 10k ohms resistors become optional.
JUNE 20, 1979

OP-100A (149-100A)  
(Etch mask 052-449A)

view from foil side

RS-15A (148-015A)  
(Etch mask 052-052-444A)

view from foil side

Serial no. up to 780699  
Use RS-15A for replacement

Serial no. up to 780699  
Use OP-100A for replacement
RS-14 (148-014)  
(Etch mask 052-445)  
view from foil side

Flat cable  
#303

Flat cable  
#303

WALTZ
SHUFFLE
SLOW ROCK
SWING
A FOX TROT  
B TANGO
BOOGIE
ENKA
BOSSANOVA
SAMBA
A MAMBO  
B CHA CHA
A BEGUINE  
B RHUMBA
SUFB2  
OO1-240
SLR-322  
OO1-231
RHYTHM A/B
RS-17 (148-017)  
(Etch mask 052-446)  
view from foil side
The GL-9 and GL-9A circuits (S/N up to S21050) are the same as the GL-9B circuit shown above except for the portions indicated by the double dotted lines, (1, 2, 3, 4). The GL-9 and GL-9A circuits for these portions are shown on page 8.
In the dotted lines shown are circuit configuration and components of VG-11 (S/N up to 780699), remainnings are almost the same as those on VG-11A which can replace the VG-11.

**OP-103A (149-103A)**
(Etch mask 052-447A)
*view from foil side*

**OP-104A (149-104A)**
(Etch mask 052-464)
Serial No. 780700 and higher
VG-11A (143-011A) (Etch mask 052-437A)
Serial No. 780700 and higher

Q501-513  2SC900-F  IC501  MC14069
Q514-532  2SC1815-QR  IC502  BA662
Q533  2SC828-R(N2)  IC503  μA78M05
Q534-535  2SA1015-Y  IC504  μA78M15
D500-526  1N1588  IC505  μA78L05

Components on foil side:
VG-11  -  R645, 0592
VG-11A -  D533

Connector cable assay
no.166
Serial No. 780700 and higher (VG-11A)
(see previous page for VG-11)
ADJUSTMENT & CHECKING

1. MASTER OSCILLATOR FREQUENCY (RHYTHM TEMPO)
   Connect an oscilloscope to Q1 collector or pin 76 on GL-9.
   1-1. Set TEMPO knob to full clockwise position (10).
       Adjust VR101 for T = 10ms.
   1-2. Turn the TEMPO control fully counterclockwise.
       Adjust VR102 for T = 10ms.
       Bottom half must be perfectly square.

   ![Waveform Diagram]
   good
   no good

2. FADE TIME
   To be adjusted after step 1 is finished.
   With rhythm (may be SAMBA-B) running, turn TEMPO fully clockwise.
   Set FADE OUT to SHORT.
   Depress START/STOP button.
   2-1. When sound becomes inaudible, count the number of LED flashes until the LED stays on steadily.
        Factory set ranges 4 (1.5sec) to 55 (2.4sec).
   2-2. To adjust, turn VR103 on GL-9.

3. RHYTHM VOICE
   Figures in the table at the right show factory standard and may be slightly deviated for personal taste or to meet frequency response of an amplifier being used.
Set all rhythm buttons to "off".
Depress START/STOP button to start the rhythm.

<table>
<thead>
<tr>
<th>VOICE to be adjusted</th>
<th>Oscilloscope</th>
<th>Frequency</th>
<th>Remark</th>
<th>Decay time</th>
<th>Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>H IN V IN</td>
<td>Adjust for</td>
<td></td>
<td>Adjust for</td>
<td>Adjust for</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ms Hz</td>
<td></td>
<td>ms</td>
<td>Vpp</td>
</tr>
</tbody>
</table>

To gate each VOICE circuit, BD through LC:
connect TS-1 to WRITE jack and tap it as necessary with INSTRUMENT SELECTOR set to the voice to be adjusted.

<table>
<thead>
<tr>
<th>BD</th>
<th>SD</th>
<th>RS</th>
<th>HH</th>
<th>CY</th>
<th>M</th>
<th>C</th>
<th>HB</th>
<th>LB</th>
<th>LC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VR57</td>
<td>16</td>
<td>62.5</td>
<td>W BALANCE set to the lowest VR58</td>
<td>100</td>
<td>-</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>3.0</td>
<td>340(Drum);</td>
<td>-</td>
<td>60</td>
<td>VR61</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>6.67</td>
<td>1480;</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Move BALANCE knob to the highest.</td>
<td>Adjusting VR60 on anyone VOICE makes all.</td>
<td>-</td>
<td>60</td>
<td>VR60</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adjusting to pin 34 on VG-11</td>
<td>-</td>
<td>350</td>
<td>VR60</td>
<td>0.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VR51</td>
<td>1.66</td>
<td>600</td>
<td>VR52</td>
<td>40</td>
<td>-</td>
<td>0.15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VR53</td>
<td>2.5</td>
<td>400</td>
<td>VR54</td>
<td>40</td>
<td>-</td>
<td>0.15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VR55</td>
<td>4.8</td>
<td>208</td>
<td>VR56</td>
<td>150</td>
<td>-</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To gate CB voice circuits, short Q527 (on VG-11) across C-E momentarily.

<table>
<thead>
<tr>
<th>CB</th>
<th>CB</th>
<th>Shift scope V IN to pin 34 on VG-11</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
<td>VR67</td>
</tr>
<tr>
<td>Q529 collector</td>
<td>VR68</td>
<td>1.8</td>
</tr>
<tr>
<td>Q530 collector</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Slide ADD VOICE knobs upward, (Tb, GU, MB, respectively). Push in CYMBAL-HIGH HAT (CANCEL VOICE) when adjusting MB.

<table>
<thead>
<tr>
<th>Tb</th>
<th>GU</th>
<th>MB</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 34</td>
<td>VR59</td>
<td>8.0</td>
<td>125</td>
</tr>
<tr>
<td>on VG-11</td>
<td>VR59</td>
<td>8.0</td>
<td>125</td>
</tr>
<tr>
<td>VR59</td>
<td>13.0</td>
<td>77</td>
<td></td>
</tr>
<tr>
<td>IC501 pin 8</td>
<td>VR64</td>
<td>0.162</td>
<td>6170</td>
</tr>
<tr>
<td>IC501 pin 4</td>
<td>VR65</td>
<td>0.178</td>
<td>5620</td>
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<tr>
<td>IC501 pin 10</td>
<td>VR66</td>
<td>0.245</td>
<td>4080</td>
</tr>
<tr>
<td>Shift scope V IN to pin 34 on VG-11</td>
<td>-</td>
<td>50</td>
<td>-</td>
</tr>
</tbody>
</table>

![Amplitude diagram](image)

![Decay time diagram](image)
PARTS LIST

ICs
179-022   µPD8048C-015   computer

There are some versions of 8048. Each has an exclusive resident program. Specify 8048C-015 for the CR-78 replacement.

179-023   AM2708P-023   ROM
020-181   µPD510LC-B   RAM
020-141   *74LS175N (TTL)
020-196   *14175B or 74C175 (MOS)
     *refer to GL-9A parts layout
020-064   µPC4558
020-180   74LS174N
020-138   74LS138N
020-124   74LS04N
020-120   74LS00N
020-084   MC14069BCP
020-041   MC14013BCP
020-169   MC14011BCP
020-160   BA-6628 VCA
020-073   µA79M15 regulator +15V
020-197   µA78M05 or µA7805 +5V
020-198   µA78L05 -5V

DIODES
018-059   1S1588
018-082   W-02 bridge 1.5A
019-013   SLP-131B LED red

SWITCHES
001-215   Power SDG-5P   100V
001-216   SDG-5P   117V
001-217   SD3-5P   220/240V
001-273   KCA10037 keyboard
001-206   HSW-0372-01-030 slide 8,16,COMBI
001-243   SRM1025 rotary MEASURE
001-242   SRM101C rotary FILL IN
001-239   SUPA2 push gang ROCK-DISCO 2
001-240   SUPB2 push gang WALTZ-2
001-231   SLR322 lever Rhythm A/B, AUTO/MANU.
001-245   SLR323 lever FADE IN/OUT
001-246   SLR323 lever MEMO/PLAY/ALL
001-241   SUP53 1push gang CLEAR, CANCEL VOICE
001-244   SRA202B rotary INSTRUMENT

081-113   Cabinet no.117
111-020   Base no.20 (foot)
072-235   Panel no.235
076-356   Name plate no.356
           rear OUTPUT-COMBI.
076-367   Name plate no.367
           rear EXT. OLOCK-WRITE
061-218   Chassis no.218 front
061-219   Chassis no.219 main
061-220   Chassis no.220 rear
061-234   Chassis no.234 sub
061-235   Chassis no.235 sub
061-236   Chassis no.236 sub

KNOBS. BUTTONS
016-043   Knob no.43 TEMPO
016-044   no.44 FILL, MEASURE.
           INSTRUMENT. ACCENT
016-080   No.80 CLEAR. CANCEL
016-081   No.81 power switch
016-048   No.48 slider
016-067   No.67 MEMORY-ALL
016-068   Button No.8 gray
016-065   No.85 white
016-086   No.86 red
016-087   No.87 green
016-088   No.88 yellow
016-089   No.89 blue

COILS. TRANSFORMERS
022-030   Coil no.30 45mH
022-031   no.31 1R
022-033   no.33 3R 700mH
022-124N  PT no.124N 100V
022-124C  PT no.124C 117V
022-124D  PT no.124D 220/240V

TRANSISTORS
017-105   28A1015-Y
017-106   28C1615-GR
017-021   28C900-F
017-046   2SC828-R (NZ) for noise
PCBs

143-011A  VG-11A (etch mask 052-437A)
142-009B  GL-9B (052-438B)
148-014   RS-14 (WALTZ-) (052-445)
148-015A  RS-15A (VARI. MEASURE)
          (052-444A)
148-017   RS-17 (PROGRAM. ROCK-)
          (052-446)
149-100A  OF-100A (052-449A)
149-103A  OF-103A (052-447A)
149-104A  OP-104A (052-464)
          (use 104A as a replacement
          for OP-129)

For the replacement, use PCBs
listed above, interchangeable
improved versions.

POTENTIOMETERS

026-024   EHHCAP25B15 100KB TEMPO
026-021   EHHCAP24B14 10KB ACCENT
029-410   LYB6B001-10KB VOL. ADD VOICE
029-411   LYB6B001-50KB BALANCE

Trimmers

028-001   EVTR4A00 (SR19) 500
028-003   EVTR4A00 (SR19) 5K
028-004   EVTR4A00 (SR19) 10K
028-005   EVTR4A00 (SR19) 20K
028-006   EVTR4A00 (SR19) 50K
028-007   EVTR4A00 (SR19) 100K

CAPACITORS

032-095   0.47mfd 35V K tant.
035-109   ECQM6103K2-600V polyester

FUSES. FUSE CLIP

008-024   SGA 0.5A prim. sec +5V 100/117V
008-026   SGA 1A sec +15V 100/117V
008-022   SGA 0.125A sec -5V 100.117V
008-053   CEE T50mA sec -5V 220/240V
008-060   CEE T250mA sec +15V 220/240V
008-062   CEE T2400mA sec +5V 220/240V
008-060   CEE T250mA prim/sec +15V 220/240V
012-003   Clip TP-758

MISCELLANEOUS

009-012   Jack SG7622
IC Sockets
012-040   ICC30-040-350G 40-pin
012-041   ICC30-024-350G 24-pin
012-042   ICC30-022-350G 22-pin
047-003   Line cord strain relief BU4801
047-023   Cord clamp 1702B
120-001   Long nut (spacer/stand off)
          no.1 3x10mm

PARTS ORDERING INFORMATION

When ordering parts, be sure to
include the following
information:

1. Model and Serial Number
2. Part Number
3. Part Name

If the necessity for a non-listed
part arises, please write
describing the parts location and
function as well as model and
serial number of the unit.
RECHARGEABLE BATTERY CHANGE

4N-100AA (5.6V) to N-SB3 (3.6V)

Serial no. up to 862999
(no name is given on the face of the battery)

Serial no. 872900 and higher
(name is definitely printed on the face)

GL-9 with 4N-100AA

1. D109 is removed at the factory to increase charging current. However, there are some products having D109 on the market. REMOVE D109 on the first occasion.

(after D109 removed)

2. Never turn on the power switch with 4N-100AA DISCONNECTED.

HIGHER voltage will ruin IC102 and IC103.

GL-9 with N-SB3

1. N-SB3 being lower in voltage can be sufficiently charged regardless of D109 existence which protects IC102 and IC103 against high voltage during an absence of N-SB3.

2. Contrary to D109, D221 and R237 are harmful to N-SB3, remove them before installing N-SB3.

IC pins and patterns misregistered
ADJUSTMENT page 15

CORRECTION
1-2. T = 10ms ------ 200ms
2-1. 4 to 55 ------ 4 to 5

VG-11A

Fulfilled part designation — not denoted or misprinted on the service notes.