NOISE GENERATOR

Despite what the average audiophile will tell you, noise can be useful. This noise generator with sample and hold facility is the basic building block for Project 80 sound effects. Design and development by Charles Blakey.

Noise sources are essential for the synthesis of many sounds. These range from musical instruments, such as pipe organ and percussive devices, to natural sounds like wind, rain and surf, and to man-made sounds such as steam engines, explosions and gunfire. The 80-12 module provides white noise, which has the characteristic hissing sound, pink noise, which is deeper in intensity, and a low frequency noise (sometimes referred to as red noise). The low frequency noise may also be used as a random modulating source.

A sample and hold circuit, also incorporated, allows external sound sources to be sampled and converted into control voltages for, say operating a VCO. The sample and hold unit, therefore, provides a means by which the synthesiser can play itself.

Noisy Networks

In this design white noise is produced by reverse biasing an NPN transistor, since this method produces a wide bandwidth. The main problem with this technique is the low amplitude of the noise and often the need to try several transistors to attain the desired amplitude. This has been largely overcome by using a two stage amplifier, IC1a and IC1b, which allows the overall gain to be varied between about 100 to 5700 times. As an additional safeguard the transistor is mounted in a socket to facilitate trying other devices, should the amplitude prove insufficient. White noise is defined as having equal energy per cycle and pink noise equal energy per octave. To derive the latter requires the white noise to be filtered at — 3 dB/octave and, since filters usually have slopes of 6 dB/octave, a 3 dB type has to be approximated. Note that other variations in noise colouration may be obtained by filtering the white or pink noise with Project 80 filters 80-6 or 80-7. The low frequency noise is obtained by low pass filtering the pink noise using a 6 dB/octave filter with a cut-off frequency of about 16 Hz (constructed around IC1d). The white and pink noise outputs will be in the range 5-10 V p-p while the low frequency noise is 10 V p-p.

The sample and hold circuit uses the principle of gating a FET, Q2, on and off and storing the sampled voltage on C16, which is buffered by voltage follower IC5b. FET gating is achieved using a CA3140E, configured as a comparator such that a positive clock pulse will cause it to go high (about 13 V) and allow the signal through to be stored on C16. When the clock pulse is near zero, IC4 will swing to about -14 V and gate the FET off. If the signal being sampled is varying rapidly in amplitude, it is essential that the clock pulse be short otherwise the output will not be in discrete steps but will follow the variations in signal amplitude while the clock pulse is high.

The internal clock in the 80-12 uses a CMOS 555 timer whose sampling rate may be varied from about 1 cycle per 0.5 S to 25 Hz. The pulse width is adjustable and the output from the clock, buffered by IC3, is available for use as, say, a synchronising trigger on an ADSR. Provision is made for using an external clock and the pulse output from the 80-2 VCO or 80-3 VCLFO is suitable.

Achieving the desired results depends on the clock rate and the amplitude of the signal being sampled. The latter may be attenuated by RV2. Additionally, when using a VCO as the clock, the pulse width is another variable for special effects.

Construction And Setting Up

Setting up the noise generator is simply achieved by adjusting PR1 to obtain the desired amplitude. This may be done in three ways: (a) using a DMM on the white noise output and adjusting PR1 until a reading of about 1V8 to 3V2 is obtained on the AC range; (b) using an oscilloscope and observing the white noise output while adjusting PR1 to obtain a peak to peak output of 5-10 V; or (c) connecting the output of the low frequency noise at R16 to a DC voltmeter and adjusting PR1 until occasional readings of about - 7 V are obtained when observed over a period of a few minutes. With most analogue meters the above readings will be approximately halved. With some transistors it may be possible to obtain the correct amplitude of the white and pink noise by increasing the gain with PR1, but the amplitude of the low frequency noise will be too high. In the latter circumstances the best approach is to try another NPN transistor rather than alter the value of R14.

Only one adjustment is required in the sample and hold section, namely, to adjust PR2 to obtain a short pulse output from the internal clock based on IC2. This adjustment should be made in the following sequence:-

a) Connect the low frequency noise output to the signal input of the sample and hold with RV2 fully clockwise. ➔

b) Connect the output of the sample and hold to a VCO with the coarse frequency control set to mid position and one of the waveforms connected to an amplifier.
c) Set RV1 (clock rate) to about 75% rotation which should give a sampling rate of about 2-3 Hz.
d) Turn PR2 fully anti-clockwise and switch power on.
e) After a few seconds delay slowly turn PR2 clockwise until the VCO output starts changing frequency in a step-wise manner.
f) Finally check that the VCO continues to change step-wise over the full range of the internal clock (RV1) and if necessary turn PR2 further clockwise until this is achieved.

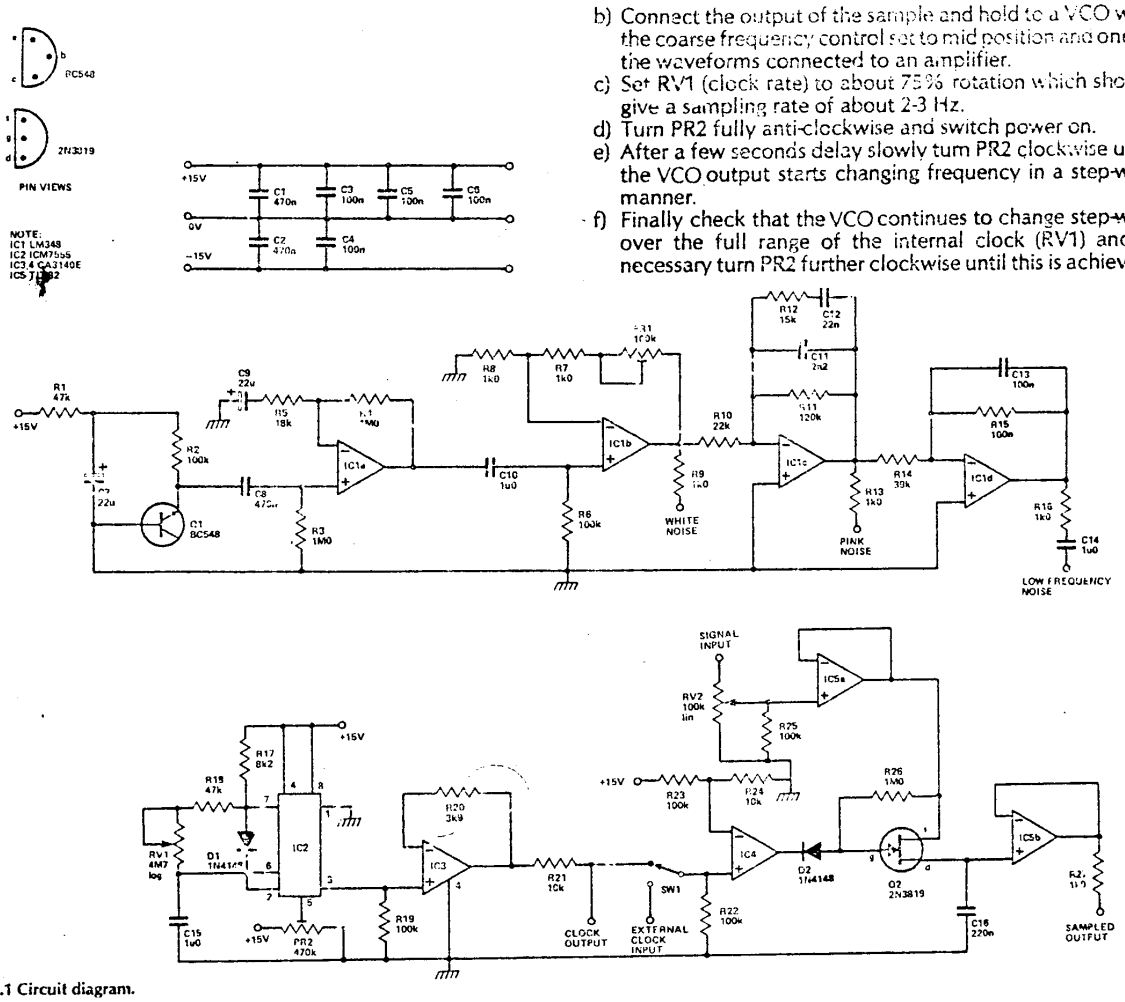

Fig.1 Circuit diagram.

HOW IT WORKS

Reverse biasing the NPN transistor, Q1, will generate noise at its base-emitter junction. The few millivolts of noise at the output of Q1 has to be amplified to the levels required for the synthesiser and this is achieved with two AC coupled non-inverting amplifiers configured around IC1a and IC1b. The gain of IC1a is fixed at about 56 while the gain of the IC1b amplifier may be adjusted from 2 to 102 by means of PR1. The overall gain of the amplifier section may, therefore, be varied from 113 to 5760 times. The amplified white noise is available via R9.

To obtain pink noise it is necessary to filter the white noise by -3 dB/octave and a close approximation over the audio range is obtained with the active filter built around IC1c. R11 and C11 form a first order low pass filter with a cut off frequency of 663 Hz, while R12 and C12 are an augmenting integrator which has an output proportional to the input signal added to an output proportional to the time integral of the input signal. The frequency response of the latter is relatively flat above about 1 kHz and below this frequency the incoming signal is attenuated at a rate of 6 dB/octave. The combination of R11/C11 with R12/C12 achieves the -3 dB/octave response and the pink noise output is available at R13. The low frequency noise is obtained by using a first order low pass filter with a cut off frequency of about 16 Hz and this is obtained with IC1d, R15 and C13 with the output being available via R16 and C14.

In the sample and hold network a signal is applied to the source of FET, Q2, via IC5a configured as a voltage follower and whose signal input may be attenuated by RV2. When Q2's gate is positive, the signal passes through and the voltage present at the signal input will change the voltage on C16 accordingly. If Q2 is gated off the last voltage on C16 is held, since leakage is kept low by buffering it with a voltage follower based on IC5b. By sampling the input for only very short durations, the voltage on C16, available at R27, will be a series of discrete steps which may in turn be used to control voltage controlled modules. The negative to positive voltage transition for gating Q2 on for sampling is obtained with IC4 configured as a comparator. With a near zero voltage at the non-inverting input of IC4 its output will be close to the negative rail voltage of -15 V and Q2 will be off. When a positive pulse is applied to the non-inverting input then IC4 goes positive (about + 13 V) and turns on Q2 so that a sample of the signal voltage can be taken and stored on C16. The internal clock used to turn Q2 on and off via IC4 is based on CMOS 555 timer, IC2. The pin configuration and operational features are the same as a bipolar 555 but the CMOS version has advantages in terms of power consumption and absence of crowbarring the power supply during the output transition. A conventional astable configuration is used and, while D1 allows a wide range of duty cycle, the main adjustment for the latter is the application of a positive voltage to its control voltage input, pin 5, via PR2. The output of the timer is buffered by IC3 so that it may be used for external synchronisation purposes. The output also goes via an SPDT switch, SW1, to comparator IC4. The switch allows external clock sources to be used.

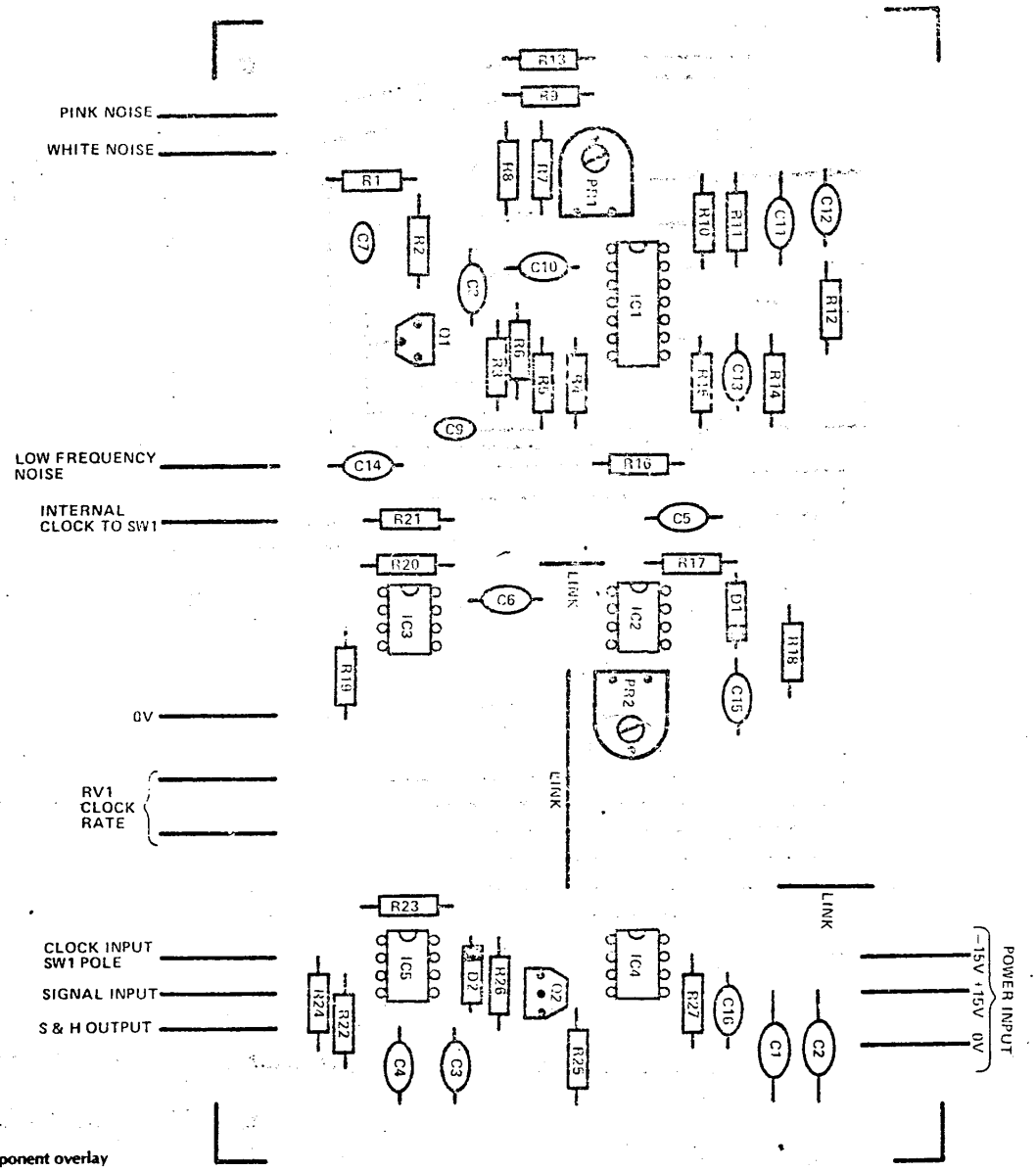

Fig.2 Component overlay

PARTS LIST

Resistors ¼ W 5% carbon		**Capacitors**		PR1	100k carbon
R1,18	47k	C1,2	470n polyester	PR2	470k carbon
R2,6,15,19,22,23,25	100k	C3,4,5,6,13	100n polyester	**Semiconductors**	
R3,4,26	1M0	C7,9	22u 25V PCB electolytic	IC1	LM348N
R5	18k	C8	470n MKH polyester	IC2	ICM7555 IPA
R7,8,9,13,16,27	1k0	C10,14,15	1u0 MKH polyester	IC3,4	CA3140E
R10	22k	C11	2n2 polystyrene	IC5	TL082 CP
R11	120k	C12	22n polycarbonate	D1, 2	1N4148
R12	15k	C16	220n MKH polyester	Q1	BC548
R14	39k			Q2	2N3819
R17	8k2	**Potentiometers/Trimmers**		**Miscellaneous**	
R20	3k9	RV1	4M7 linear	SW1	SPDT miniature toggle
R21,24	10k	RV2	100k linear	Transistor holder	

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SAMPLE & HOLD